WHAT IS CLAIMED IS :

1. A hardware stack, comprising:

an instruction decoder for generating a plurality of decoding signals, each of the plurality of decoding signals denoting one of a plurality of stack operations;

a stack storage comprising a plurality of storage locations, each of the plurality of storage locations being classified into one of at least two banks; and

a stack pointer circuit for pointing to at least one of the stack banks of the stack storage in response to at least one decoding signal to thereby cause a stack operation.

2. A digital data processor, comprising:

an instruction decoder for decoding an instruction and generating a plurality of decoding signals;

a stack storage comprising a plurality of locations for storing stack items;

a stack pointer for pointing to at least one of the locations of said stack storage; and

a stack storage control circuit responsive to the decoding signals, for one of inserting a one-word item into said stack storage and removing a two-word item from said stack storage, based on a content of said stack pointer.

3. The digital data processor of claim 2, wherein each location of said stack storage is configured for storing a one-word item.

4. The digital data processor of claim 3, wherein a two-word item is one of inserted into and removed from two adjacent locations of said stack storage at a ~~given~~ time.

5. The digital data processor of claim 4, wherein said stack storage control circuit one of increases and decreases the content of said stack pointer by one when the decoding signals indicate a one-word stack operation; and wherein said stack storage control circuit one of increases and decreases the content of said stack pointer by two when the decoding signals indicate a two-word stack operation.

6. A digital data processor, comprising:

a stack storage including a plurality of locations, wherein each of the locations of said stack storage are assigned to one of a first bank and a second bank;

a main stack pointer for pointing to a location of said stack storage;

a first bank stack pointer for pointing to a location assigned to said first bank;

a second bank stack pointer for pointing to a location assigned to said second bank;

an instruction decoder for decoding a stack-based instruction and generating a plurality of decoding signals, each of the plurality of decoding signals denoting one of a one-word push operation, a one-word pop operation, a two-word push operation and a two-word pop operation; and

a stack pointer control logic circuit for controlling said first and second bank stack pointers in response to the decoding signals such that at least one of a one-word item and a two-word item is one of inserted into and removed from said stack storage based on a content of said main stack pointer.

7. The digital data processor of claim 6, wherein said stack storage comprises 2^{n+1} locations, n being a positive integer, and wherein the first band and the second bank each include 2^n locations.

8. The digital data processor of claim 6, wherein one of the first and second banks includes locations with addresses having a least significant bit of logic '0' and the other of the first and second banks includes locations with addresses having a least significant bit of logic '1'.

9. The digital data processor of claim 6, wherein said stack pointer control logic circuit includes:

an adder for adding one of a plurality of predetermined integers to a content of said main stack pointer in response to a first decoding signal from said instruction decoder;

a first selector for selecting for output one of the content of the main stack pointer and a content of said adder in response to a second decoding signal from said instruction decoder, wherein the output of said first selector comprises a high-order bit portion and a low-order bit portion;

a first control logic for generating a first control signal in response to the low-order bit portion of the output from said first selector and a third decoding signal from said instruction decoder;

a second control logic for generating a second control signal in response to the low-order bit portion of the output from said first selector and a fourth decoding signal from said instruction decoder;

an increment logic for incrementing the high-order bit portion of the output from said first selector;

a second selector for selecting one of the high-order bit portion of the output from said first selector and the output of said increment logic in response to the first control signal; and

a third selector for selecting one of the high-order bit portion of the output from said first selector and the output of said increment logic in response to the second control signal;

wherein the outputs of said second and third selectors are provided to said second and first bank stack pointers, respectively.

10. The digital data processor of claim 9, wherein said plurality of predetermined integers ~~includes~~ include one of +1, +2, -1 and -2; and wherein said increment logic increments the high-order bit portion of the output from said first selector by one.

11. The digital data processor of claim 9, wherein said main stack pointer is updated by the content of said adder.

12. The digital data processor of claim 9, wherein said low-order bit portion of the output from said first selector comprises the least significant bit of the output from the first selector.

13. The digital data processor of claim 12, wherein said first and second control logics alternately enable said second and third selectors, respectively, based on logic states of the least significant bit of the output from the first selector, during the one-word push and pop operations.

14. The digital data processor of claim 13, wherein said second selector is enabled when the least significant bit of the output from ~~the~~ said first selector is logic '1'.

15. The digital data processor of claim 13, wherein said third selector is enabled when the least significant bit of the output from said first ~~selector's output~~ selector is logic '0'.

16. The digital data processor of claim 12, wherein said first and second control logics enable both of said second and third selectors, irrespective of logic states of the least significant bit of the output from said first selector, during the two-word push and pop operations.

17. The digital data processor of claim 6, wherein said stack pointer control logic circuit comprises:

an adder adds one of a plurality of predetermined integers to a high-order bit portion of a content of said main stack pointer in response to a first decoding signal from said instruction decoder;

a control logic for generating one of a first, second, third, and fourth control signals, and combination thereof, in response to a low-order bit portion of the content of said main stack pointer and a second decoding signal from said instruction decoder;

a first selector for selecting one of the high-order bit portion of the content of said main stack pointer and an output of said adder in response to the first control signal;

a second selector for selecting one of the high-order bit portion of the content of said main stack pointer and the output of said adder in response to the second control signal; and

a third selector for selecting one of the high-order bit portion of the content of said main stack pointer and the output of said adder in response to the third control signal;

wherein outputs of said second and third selector are provided to said second and first bank stack pointers, respectively, and the low-order bit portion of the content of said main stack pointer is controlled by the fourth control signal.

18. The digital data processor of claim 17, wherein the plurality of predetermined integers ~~comprises~~ comprise +1 and -1.

19. The digital data processor of claim 17, wherein said high-order bit portion of the content of said main stack pointer is updated by the content of said adder.

20. The digital data processor of claim 17, wherein said low-order bit portion of the content of said main stack pointer comprises a least significant bit of the content of said main stack pointer.

21. The digital data processor of claim 20, wherein said control logic alternately enables said second and third selectors, based on logic states of the least significant bit of the content of said main stack pointer, during the one-word push and pop operations.

22. The digital data processor of claim 21, wherein said second selector is enabled when the least significant bit of the content of said main stack pointer is logic '1'.

23. The digital data processor of claim 21, wherein said third selector is enabled when the least significant bit of the content of said main stack pointer is logic '0'.

24. The digital data processor of claim 17, wherein said control logic enables both said second and third selectors, irrespective of logic states of the least significant bit of the content of said main stack pointer, during the two-word push and pop operations.

25. The digital data processor of claim 20, wherein said control logic toggles the least significant bit of the content of said main stack pointer during the one-word push and pop operations.